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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,038	09/24/2003	Frankie F. Roohparvar	400.021US02	5054

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LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,038	ROOHPARVAR ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Le et al PN 5,727,005.

In regards to claim 1: Le et al teaches a method for writing data to a boot area (Boot Region Column 22 line 43 to Column 23 line 31) of a synchronous memory device (Column 16 lines 3-19), the method comprising: initiating a write operation to the boot area (Column 1 lines 37-53 WE and Column 22 line 43 to Column 23 line 31); reading data from a register circuit (212 or alternatively 61); and authorizing the write operation to the boot area if the data is in a first state (a match that write is authorized via 231 or 64 respectively).

In regards to claim 2: Le teaches checking a status of a detection circuit (224 or alternatively 63) if the data is in a second state (write is enabled); and authorizing the write operation to the boot area based on an output of the detection circuit.

In regards to claim 3: Le teaches the detection circuit monitors an externally provided signal (address and attributes) to the memory device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al PN 5,727,005 in view of Kynett et al PN 5,249,158.

In regards to claim 4: Le teaches write protection of a boot area of a synchronous memory as described above. Le also teaches write protection of any selected region. Le does not teach the structure of the synchronous memory or that the boot area is top bootable or bottom bootable. Kynett et al teaches a synchronous memory in which both top booting and bottom booting are supported (Column 8 lines 43-65). It would have been obvious to have Le's synchronous memory include both top booting and bottom booting because this would have allowed for greater system compatibility.

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al PN 5,727,005 in view of Johnson et al PN 5,343,437.

In regards to claims 8-9: Le teaches the write protection of a boot area of a synchronous memory as described above. Le however does not expressly teach he option register is copied from a non-volatile memory upon system power up. Johnson et al teaches copying data from a non-volatile memory to a volatile memory upon system power up. It would have been obvious

to copy the options from a non-volatile memory to a volatile memory upon power up because the volatile memories are faster than non-volatile memories.

6. Claims 1-3, 5 are ejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al PN 5,991,197.

In regards to claims 1, 5: Ogura et al teaches a method for writing data to a boot area (1a or alternatively 102a) of a synchronous memory device (Figure 1 or alternatively Figure 13), the method comprising: initiating a write operation to the boot area (write or erase); reading data from a circuit (2 or alternatively 102); and authorizing the write operation to the boot area if the data is in a first state (Bit not locked). Ogura et al does not teach the lock bits being stored in a register. Official notice is taken that registers are well known. It would have been obvious to store the lock bits in a register because this would have freed up memory array space and increased ease in accessing.

In regards to claim 2: Ogura et al teaches checking a status of a detection circuit (8 or alternatively 103) if the data is in a second state (write is enabled); and authorizing the write operation to the boot area based on an output of the detection circuit.

In regards to claim 3: Ogura et al teaches the detection circuit monitors an externally provided signal (CE, RP, WP) to the memory device.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al PN 5,991,197 in view of Kynett et al PN 5,249,158.

In regards to claim 4: Ogura teaches write protection of a boot area of a synchronous memory as described above. Ogura also teaches write protection of any selected region. Ogura does not teach the structure of the synchronous memory or that the boot area is top bootable or bottom bootable. Kynett et al teaches a synchronous memory in which both top booting and bottom booting are supported (Column 8 lines 43-65). It would have been obvious to have Ogura's synchronous memory include both top booting and bottom booting because this would have allowed for greater system compatibility.

8. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al PN 5,991,197 in view of Johnson et al PN 5,343,437.

In regards to claim 6-9: Ogura et al teaches the write protection of a boot area of a synchronous memory as described above. Ogura et al however does not expressly teach he Lock bits being transferred to volatile memory upon system power up. Johnson et al teaches copying data from a non-volatile memory to a volatile memory upon system power up. It would have been obvious to copy the Lock bits to a volatile memory from the non-volatile memory upon power up because the volatile memories are faster than non-volatile memories.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
May 24, 2005

PAUL R. MYERS
PRIMARY EXAMINER